



**UNITED STATES DEPARTMENT OF COMMERCE**  
**Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
-----------------	-------------	----------------------	---------------------

09/023,234    02/13/98    HOLMAN

T    042390P5658

LM01/0602  
BLAKELY SOKOLOFF TAYLOR & ZAFMAN  
12400 WILSHIRE BOULEVARD 7TH FLOOR  
LOS ANGELES CA 90025

EXAMINER
----------

VERBRUGGE, K	
ART UNIT	PAPER NUMBER

2751  
DATE MAILED:

U  
06/02/00

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

*See attached final Office action.*

# Office Action Summary

Application No.  
09/023,234

Applicant(s)

Holman

Examiner  
Kevin Verbrugge

Group Art Unit  
2751



☒ Responsive to communication(s) filed on Mar 2, 2000

☒ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

## Disposition of Claim

☒ Claim(s) 1-17 is/are pending in the application

Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration

☐ Claim(s) \_\_\_\_\_ is/are allowed.

☒ Claim(s) 1-17 is/are rejected.

☐ Claim(s) \_\_\_\_\_ is/are objected to.

☐ Claims \_\_\_\_\_ are subject to restriction or election requirement.

## Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on \_\_\_\_\_ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some\* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) \_\_\_\_\_

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\*Certified copies not received: \_\_\_\_\_

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 8

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

Art Unit: 2751

**DETAILED ACTION**

***Response to Amendment***

This final Office action is in response to Amendment A, paper #9, filed 3/2/00, which amended claims 1-3, 5-9, and 14-17. Claims 1-17 remain pending. All objections and rejections not repeated below are withdrawn. Applicant's arguments have been considered but are moot in view of the new grounds of rejection.

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 7, 8, 12, and 14-17 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 4,045,781 to Levy et al., hereinafter simply Levy.

Regarding claims 1, 2, and 17, Levy shows the claimed memory module as memory module 30 in Fig. 1. Memory module 30 includes

Art Unit: 2751

the claimed plurality of memory devices as low stack 0-3 and high stack 0-3. Furthermore, memory module 30 includes the claimed memory module controller as memory transceiver 41 and memory control and timing unit 42. This controller receives a first memory transaction in a first format from a first memory bus (memory bus 40) and converts the first memory transaction into a second memory transaction in a second format for the plurality of memory devices as claimed. The second memory transaction is clearly different from the first memory format since the outputs of memory transceiver 41 and memory control and timing unit 42 are clearly different from their inputs. This is indicated by the differing nature of the signal lines shown in Fig. 1 and by the other figures and disclosure.

Regarding claim 3, Levy shows the claimed second memory bus as the signal lines coming out of memory transceiver 41 and memory control and timing unit 42.

Regarding claim 4, Levy's second memory bus includes the claimed address, data, and control signal lines as shown in Fig. 1.

Art Unit: 2751

Regarding claim 5, Levy's second memory bus includes the claimed signal line for a clock signal (timing signal) as shown in Fig. 1.

Regarding claim 7, Levy's memory buses clearly have different numbers of signal lines as shown by Fig. 1.

Regarding claim 8, Levy shows the claimed request handling circuitry as memory transceiver 41 and shows the claimed control logic as memory control and timing unit 42.

Regarding claim 12, Levy teaches that his memory devices are volatile, as claimed, since they are traditional random access memory devices.

Regarding claim 14, Levy does not explicitly mention the claimed handshake signal, however it is inherent in his device since his memory controller necessarily communicates data to the system memory controller (memory management unit 22). It is clear that the memory module controller communicates data and control signals to the system memory controller since the data (D) and control (C) lines of memory bus 40 are bidirectional.

Art Unit: 2751

Regarding claims 15 and 16, Levy teaches that his device performs the claimed reads and writes.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6, 9, 10, 11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,045,781 to Levy et al., hereinafter simply Levy.

Regarding claim 6, Levy does not teach that his memory buses operate at different rates, however it would have been obvious to one skilled in the art at the time of the invention to operate them at different rates since they carry different signals and have different lengths, virtually ensuring that the maximum data rate of each one would be different.

Art Unit: 2751

Regarding claim 9, Levy shows separate address and data lines for both his first and second memory buses. He does not teach that his first memory bus carries time-multiplexed data and address information as claimed, however it would have been obvious to one skilled in the art to time-multiplex the first address bus to save signal lines and their associated cost and space.

Regarding claims 10, 11, and 13, Levy does not teach that his memory modules have the claimed characteristics, however it would have been obvious to the skilled artisan at the time of the invention to implement Levy's memory modules as SIMMs, DIMMs, or nonvolatile memory devices, as appropriate, depending on design considerations, since all three types of devices were well-known to the artisan.

### ***Conclusion***

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2751

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon (U.S. Patent 5,357,621 to Cox) is considered pertinent to Applicant's disclosure.

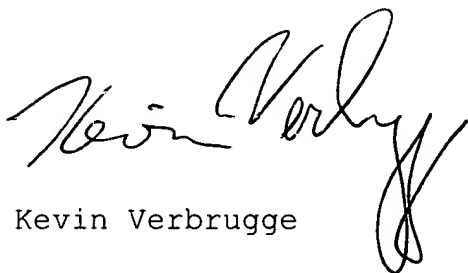
Any inquiry concerning this or an earlier communication from the Examiner should be directed to Kevin Verbrugge by phone at (703) 308-6663.

Any response to this action should be mailed to Box AF, Commissioner of Patents and Trademarks, Washington, D.C. 20231 or faxed to (703) 308-9051 or -9052 and labeled "OFFICIAL" or "UNOFFICIAL" as appropriate. Hand-delivered responses should be



Art Unit: 2751

brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA.,  
Sixth Floor (Receptionist).

A handwritten signature in cursive script, appearing to read "Kevin Verbrugge". The signature is written in dark ink and is positioned above the printed name and title.

Kevin Verbrugge

Patent Examiner

May 25, 2000